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PATENT Atty. Docket No. 28944/40163

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Robbe et al.)
Serial No.: 10/556,647) CERTIFICATE OF TRANSMISSION)
Filed: November 10, 2005	I hereby certify that this paper and any papers referred to herein, is/are being facsimile transmitted to the Mail Stop AF, Commissioner
Title: Voltage Shift Control Circuit for PLL	for Patents, U.S. Patent office, facsimile number 571-273-8300 on the following date:
Group Art Unit: 2816) February 9, 2009
Examiner: Khareem E. Almo	} I Starte for
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Pre-Appeal Brief Request for Review

Mail Stop AF Commissioner for Patents P.O. Box 1450 Alexandria, VA 223130-1490

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In response to clear errors of fact in the Office action dated August 7, 2008, please consider the following arguments in support of a Pre-Appeal Brief Request for Review. In rejecting claims 1, 7, and 10-14 under 35 U.S.C. §103(a) as obvious over Fan (US6693494) in view of page 227 of Nilsen and Riedel, the examiner states on page "[Fan] fails to disclose at least one series voltage shift capacitor. Figure 6.17 of Riedel teaches the use of 3 series capacitors to replace one capacitor. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to use a number of capacitors in series for one a (sic) larger capacitor for the well known purpose of optimizing the value of the capacitance."

From this statement, it is clear that the examiner is misinterpreting the claim limitation in claim 1 "... at least one series voltage shift capacitor coupling the phase comparator and the voltage controlled oscillator of a phase locked loop ..." The quoted language from claim 1 clearly states that the capacitor is in series with and between the phase comparator and the voltage controlled oscillator of a phase locked loop. This is how a person of ordinary skill would interpret the language from claim 1.

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There is no other rational interpretation of the above quoted limitation in claim 1 than the capacitor both couples the phase comparator and the voltage controlled oscillator and is in series with these circuits. There is no alternative interpretation that would be understood by one of ordinary skill in this art.

Fan does not disclose any capacitors that are in series between the phase comparator and the voltage controlled oscillator. The examiner recognizes this but seems to read the terms "series capacitor" as used in the context of claim 1 as merely being multiple capacitors connected in series to each other and not as a capacitor connected in series between two specific circuits. The latter is the understanding that a person of ordinary skill in the circuit art would have of the words of claim 1. This was pointed out to the examiner in the response after final.

In the advisory action, the examiner briefly states "C1 and C3 are series capacitors coupling the phase comparator and the VCO as stated in the rejection." In Figure 6, capacitors C1 and C3 are clearly connected to ground and would be considered as "parallel capacitors" by one of ordinary skill in the art. Also, no where in the description of Fan is there any disclosure to support the examiner's assertion that either capacitor C1 or C3 are in series with and coupling the phase comparator and the VCO.

Conclusion

The examiner's interpretation of claim 1 is without basis and contrary to how claim 1 would be interpreted by one of ordinary skill in the art. Fan does not disclose or suggest the present claimed invention either alone or in combination with the other cited documents. Therefore, all claims are allowable over the art of record and this application should be passed to issue.

Respectfully submitted,

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February 9, 2009

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